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FOR

**MULTI-LAYER FILM STACK FOR EXTINCTION OF SUBSTRATE
REFLECTIONS DURING PATTERNING**

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**MULTI-LAYER FILM STACK FOR EXTINCTION OF SUBSTRATE
REFLECTIONS DURING PATTERNING**

BACKGROUND

Field of the Invention

[0001] The invention relates to integrated circuit fabrication and, more particularly, to the definition and alignment of interconnections in integrated circuit structures.

Background

[0002] Modern integrated circuits use interconnections to connect the individual devices on a chip or to send and/or receive signals external to the chip. Popular types of interconnections include aluminum or copper interconnections (lines) coupled to devices, including other interconnections (lines) by interconnections through vias.

[0003] Fabricating an interconnection structure to a device formed on a circuit substrate, such as an interconnection to a transistor device, typically involves introducing a photoimageable material (e.g., photoresist) over a dielectric layer insulating the device. The photoimageable material is patterned to have an opening to the dielectric above the desired point of contact for the subsequent interconnection. An etch is then used to form an opening or via through the dielectric layer to the device.

[0004] One problem with the current state of the art photoimaging technique is the formation of undesired openings in the photoimageable material due to substrate reflections of light. **Figure 1** illustrates the light scattering effect according to conventional processing. **Figure 1** shows structure 100 including substrate 110 of, for example, a semiconductor material such as silicon. Substrate 110 has, in this example, transistor devices 120 formed in active areas of the substrate. The active areas are separated from one another by shallow trench isolation (STI) 130. Dielectric material 135 such as, for example, silicon dioxide (SiO_2) overlies devices 120 and substrate 110. Photoimageable material 140 such as a positive photoresist overlies dielectric material 135. In this example, an opening in photoimageable material is desired over area 150 which will be an opening for a via to transistor device 120.

[0005] Referring to **Figure 1**, it is shown that light directed through opening area 150 in the process of developing the photoimageable material may scatter within structure 110 and reflect off structures on substrate 110 (i.e., substrate reflections). Certain structures, such as gate electrodes and STI 130 are sufficiently reflective to reflect the scattered light and create undesired developed areas in photoimageable material 140. **Figure 1** shows undesired opening area 180 formed by reflective light 160 off a gate electrode and reflective light 170 off STI 130. Upon developing the photoimageable material, the undesired opening area 180 may be developed in such a way to create an opening to photoimageable material to dielectric material 135.

[0006] By creating undesired openings in the photoimageable material, failure modes are introduced into the circuit device processing. When these openings are later filled with interconnection material, electrical shorts may be introduced either between metal lines or on the silicon structure. Further, undesired interconnects coupled to silicon surface introduce a capacitive element in the structure.

[0007] Attempts to remedy the problem of creating undesired opening areas include placing an anti-reflective coating over the structure. Such technique, however, involves introducing an additional film which adds process cost and complexity and possibly additional defects in the process flow. Reduction of the light intensity is not a workable solution at this point as it requires approximately 27 milliJoules (mJ) to develop positive photoresist with only one to two milliJoules margin. Therefore, reducing the light intensity may result in the loss of the desired opening area, such as opening area 150.

[0008] What is needed are improved processing techniques and an improved structure that suppresses undesired reflections.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] **Figure 1** shows a schematic, cross-sectional view of a portion of a prior art integrated circuit substrate and illustrates light reflections through a photoimageable material opening.

[0010] **Figure 2** shows a cross-sectional view of a portion of an integrated circuit structure including a substrate having circuit devices formed thereon, an etch stop layer overlying the substrate followed by a base dielectric material and two alternating layers of dielectric material according to an embodiment of the invention.

[0011] **Figure 3** shows the structure of **Figure 2** after the introduction of two additional alternating layers of dielectric material.

[0012] **Figure 4** shows the structure of **Figure 3** after the introduction of two additional alternating layers.

[0013] **Figure 5** shows the structure of **Figure 4** after the introduction of three additional alternating layers.

[0014] **Figure 6** shows the structure of **Figure 5** after the introduction and patterning of a photoimageable material having openings to devices in the substrate.

[0015] **Figure 7** shows the structure of **Figure 6** after introducing an interconnection to a contact point on the substrate.

[0016] **Figure 8** is a graphical representation of the peak reflectance through a prior art substrate structure and a structure according to **Figure 5**.

DETAILED DESCRIPTION OF THE INVENTION

[0017] The invention relates to techniques and an apparatus for forming interlayer dielectric material layers that suppress undesired substrate reflections. In

one embodiment, a method includes introducing a dielectric layer over a substrate between an interconnection line and a contact point, the dielectric layer comprising a plurality of different material layers, and patterning an interconnection to the contact point. An embodiment of the apparatus includes a substrate comprising a plurality of devices formed thereon and a dielectric layer comprising a plurality of alternating material layers overlying the substrate. The apparatus also includes an interconnection line overlying the dielectric layer and coupled to at least one of the plurality of devices.

[0018] **Figures 2-7** illustrate an example of a dielectric layer that suppresses substrate reflections. Unless otherwise specified, substrate refers to the device substrate, such as a silicon semiconductor substrate as well as a substrate having one or more interconnection lines formed thereon. In the latter case, the dielectric layer described herein is an interlayer dielectric material(s) between interconnection lines. It is recognized that the majority of substrate reflection problems occur through the primary dielectric material over the device substrate (e.g., primary dielectric material between the device substrate and the first interlayer dielectric layer). Accordingly, with reference to **Figure 2** through **Figure 7**, a technique is shown of forming an interlayer dielectric over the device substrate. It is appreciated that subsequent dielectric material layers (i.e., subsequent interlayer dielectric material layers) may optionally be formed according to technique described herein, depending in part on the extent of reflections seen at the various higher levels.

[0019] **Figure 2** shows structure 200 including device substrate 210 of, for example, a semiconductor such as silicon. Device substrate 210 includes a plurality of devices 220 formed in active areas thereon. Such active areas are defined, in one sense, by isolation structures such as shallow trench isolation (STI) structures 230.

[0020] Overlying substrate 210 and any devices formed thereon is etch stop layer 240. In one embodiment, etch stop layer 240 is, for example, silicon nitride material deposited by chemical vapor deposition to a thickness on the order of about 500 angstroms (\AA). In one sense, etch stop layer 240 protects substrate 210 and devices formed thereon from a subsequent etching operation.

[0021] Referring to **Figure 2** overlying etch stop layer 240 is base layer 250. Base layer 250 is, for example, silicon dioxide (SiO_2) formed by tetraethyl orthosilicate (TEOS) or a plasma enhanced chemical vapor deposition (PECVD) source. In one embodiment, base layer 250 is doped with phosphorous or boron (e.g., by adding PH_3 or B_2H_6 during deposition) so that base layer 250 may serve as a getter (collector) of metallic contaminants.

[0022] It is appreciated that the introduction of base layer 250 over the substrate may proceed in a conformal manner leaving a non-planar substrate surface. In such cases, following the introduction and possible doping of base layer 250, structure 200 is planarized by, for example, the use of a chemical-mechanical polish. A representative thickness of planarized base layer 250 of, for example, silicon dioxide, is on the order of 1900 angstroms (\AA).

[0023] It is generally desirable at this point to introduce a dielectric cap over planarized base layer 250. The dielectric cap is included, in one sense, to mask any microdefects caused by the planarization. Referring to **Figure 2**, in this embodiment, dielectric cap 255 includes a plurality of alternating material layers. **Figure 2** shows dielectric cap 255 of a first dielectric material 260A and a different second dielectric material 270A. In one embodiment, dielectric material 260A is silicon oxynitride deposited to a thickness on the order of 50 Å. Dielectric material 270A is, in one embodiment, silicon dioxide deposited to a thickness on the order of about 283 Å.

[0001] One objective of introducing dielectric cap 255 over base layer 250 is to yield a uniform interlayer dielectric film. One way to target a uniform film of dielectric cap 255 is by introducing the cap layers on a multi-station tool such as a Concept 2 Sequel™, commercially available from Novellus Systems, Inc. of San Jose, California. Through the use of a multi-station tool, it is possible to introduce multiple alternating layers or films of dielectric material as dielectric cap 255. **Figure 3** shows two layers or films 260A and 260B of silicon oxynitride deposited to approximately 50 Å each. Disposed between each silicon oxynitride layer or film (i.e., between layer or film 260A and 260B) are dielectric layers or films 270A and 270B of silicon dioxide introduced to a thickness on the order of about 283 Å. **Figure 4** shows three alternating layers or films of silicon oxynitride (260A, 260B, and 260C) and three layers or films of silicon dioxide (270A, 270B, and 270C). **Figure 5** shows six layers or films of silicon oxynitride

(260Å-260F) and six layers or films of silicon dioxide (270Å-270F).

[0025] By using a multi-station tool to introduce dielectric cap 255, multiple alternating layers or films of different dielectric materials may be introduced efficiently. By selecting thicknesses of the alternating materials and the number of alternating films, cap layer 255 may be maintained within a suitable thickness range consistent with prior art structures. For example, in one embodiment, it is desired that a dielectric cap 255 has a thickness on the order of about 2,000 Å for the structure described (i.e., an overall dielectric thickness (cap + base layer + etch stop) of approximately 4,000 Å).

[0026] The structure represented in each of **Figure 2** through **Figure 5** has silicon dioxide as the ultimate layer or film and for each film thickness of the alternating layers or films, the silicon dioxide film is more than five times thicker than the silicon oxynitride film. With the selection of the alternating cap materials as silicon dioxide and silicon oxynitride, one reason it is desired to have silicon dioxide as the ultimate layer or film in the multi-layer stack is that silicon dioxide is generally a much harder material than silicon oxynitride. Accordingly, any subsequent polishing steps associated with the introduction of, for example, interconnection material over dielectric cap 255 allows for planarization (e.g., polishing) of silicon dioxide rather than silicon oxynitride. Silicon dioxide also provides better adherence to a subsequent interconnection structure such as an interconnection line of aluminum or copper.

[0027] One reason for selecting films of silicon dioxide that are more than five times thicker than the

silicon oxynitride counterparts is that silicon oxynitride has a higher dielectric constant than silicon dioxide. Measurably increasing the dielectric constant of dielectric cap 255 may impair circuit performance by, for example, introducing undesired capacitance, such as metal to metal capacitance within the structure.

[0028] It has been observed that with a dielectric cap that is a two layer or film of 1,000 Å of silicon oxynitride and 1,000 Å of silicon dioxide (one to one relationship) with undesired substrate reflections from, for example, STI 231, are inhibited. Reduction of the amount of silicon oxynitride to silicon dioxide from one to one, to one to five or one to six inhibits some undesired reflections but is not as effective as the inhibiting reflectance of the one to one relationship. It has also been observed by interweaving or alternating the silicon oxynitride and silicon dioxide films as described above using significantly less silicon oxynitride, similar reflection inhibition to the one to one relationship is seen. Therefore, interweaving or alternating as described the structure shown, for example, in **Figure 5**, is suitably effective at inhibiting light reflection while minimizing device performance issues while using silicon oxynitride as a portion of dielectric cap 255.

[0029] **Figure 6** shows the structure of **Figure 5** after the introduction and patterning of photoimageable material 280. In one embodiment, photoimageable material 280 is a positive photoresist. Photoimageable material 280 is patterned to have opening areas 290 over the dielectric structure, the opening areas formed in this example to devices 220 on substrate 210. **Figure 5** also illustrates minimal undesired developed areas (none) in photoimageable

material 280 as a result of undesired reflections in forming opening areas 290. **Figure 7** shows the structure of **Figure 6** after the etching of openings to devices 220 on substrate 210 and the removal of photoimageable material 280. **Figure 7** also shows the structure after the introduction of interconnection material 295 to devices 220 and interconnection material 297 over the dielectric layer. Such etching, removal of photoimageable material, and introduction of interconnection material may proceed by techniques as known in the art.

[0030] Although the embodiment shown in **Figure 6** illustrates no undesired opening areas due to substrate reflection, it is appreciated that the total inhibition of substrate reflection depends also on the light that is reflected. It is appreciated that in forming an opening area in, for example, photoresist material, light of possibly many wavelengths is introduced into the substrate. In this sense, the path length that the light travels is also significant in determining substrate reflections. For example, where the path length dictates that the wavelength will be modified by one-half, it is possible that such wavelength difference will be destructive and not contribute to a noticeable reflection. On the other hand, if the reflected light differs from the introduced light by a full wavelength, it is possible that such reflective light will be constructive and lead to undesired developing of photoimageable material. Thus, a complete inhibition of substrate reflections according to the techniques described herein is difficult to achieve in every case. Nevertheless, the structure described herein and the techniques of forming such structure offer an improvement over prior art techniques. **Figure 8** shows the simulated peak reflectance of a prior art dielectric

material configuration such as described with respect to **Figure 1** and the accompanying text yielding a peak reflectance of approximately 66 percent. The structure shown in **Figure 6**, on the other hand, has a peak reflectance of 24 percent.

[0031] In the above embodiment, a dielectric cap of interweaved layers or films of dielectric materials of silicon dioxide and silicon oxynitride is presented. It is appreciated that there may be other materials besides silicon dioxide and silicon oxynitride that may suitably substituted. Other materials may likewise be substituted for the base layer material as well. These dielectric materials include materials having a dielectric constant lower than silicon dioxide ("low k" dielectrics).

[0032] In the preceding detailed description, an improved interlayer dielectric is presented that inhibits substrate reflections. The invention is described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.